

Registration No:

--	--	--	--	--	--	--	--	--	--

Total Number of Pages: 02 bput question papers visit <http://www.bputonline.com>M.TECH  
P2SPBC01

**2<sup>nd</sup> Semester Regular Examination 2016-17**  
**DSP Algorithm & Architectures**  
**BRANCH: SIGNAL PROCESSING AND ENGG.**

Time: 3 Hours

Max Marks: 100

Q.CODE: Z361

**Answer Question No.1 which is compulsory and any FOUR from the rest.**  
**The figures in the right hand margin indicate marks.**

**Q1** Answer the following questions: *Short answer type* (2 x 10)

- Add 111222 with 112222 in Redundant Number System.
- How Pipelining and Parallel Processing improves speed and power of a sequential system?
- How over flow can be eliminated in Fixed Point Processor?
- What is the use of Sign Extension in parallel multiplication?
- Express carry recurrence ( $c_{i+1}$ ) in terms of  $g_i, c_i, p_i, t_i$ .
- Compare bit-parallel, bit-serial and digital-serial system.
- What is node scheduling and node projection?
- Compute the loop bound of the following loops and state the critical loop and its iteration bound.

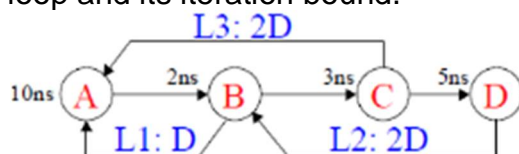


Figure 1

- Design a full adder in terms of half adder.
  - $R_{x^2+2}[5x^2 + 3x + 5] = ?$
- Q2**
- Explain the 4 types of graphical representation of DSP algorithm, with proper example. (10)  
bput question papers visit <http://www.bputonline.com>
  - What is retiming, explain with an example. Explain the properties of retiming with suitable examples. (10)
- Q3**
- What is Quantization error? In the ADC derive how SNR is dependent on number of bits and variance. (10)
  - A 3<sup>rd</sup> order inner product defined by the convolution sum  $y = \langle c, x \rangle = \sum_{n=0}^3 c[n]x[n]$  for the given co-efficient  $c[0] = -2, c[1] = 3, c[2] = 1$ . The values of  $x[k]$  are  $[0] = 1, x[1] = -3, x[2] = 7$ . Assume the data is given N=4 bit 2's complement encoding. Find out the LUT and the output y. (10)
- Q4**
- Implement Shift-Adder Distributed architecture (DA). How speed can be increased and the size can be reduced for DA architecture? (10)

- b)** Write down the algorithm for Canonic Signed Digit (CSD) conversion. **(10)**  
Write two properties of CSD numbers.  
Compute the carry free addition of  $29_{10} = 100\bar{1}01_{SD}$  to  $-9_{10} = 0\bar{1}1\bar{1}11_{SD}$  in SD system.
- Q5 a)** Derive the condition for no carry propagation in Redundant Number System. **(10)**  
For (3,0,5) add 243 with 435 such that no carry will propagate.
- b)** Write down the binary division algorithm. Divide  $(41)_{10}$  by  $(7)_{10}$  for  $n=3$ . **(10)**
- Q6 a)** Derive the relationship between scheduling vector and basis vector, for broadcasting & pipelining variable. **(10)**
- b)** Obtain the design for FIR filter using Horner's rule for Broadcast input and Pipelined output. Draw the DAG for digital FIR filter and Processor Element. **(10)**
- Q7 a)** Write the algorithm for LFSR. Write down the VHDL code for LFSR of length 6. **(10)**
- b)** Write down Winograd Algorithm. Construct a  $2 \times 2$  convolution algorithm using the Winograd algorithm with  $m(p) = p(p-1)(p+1)$ . **(10)**