Registration No: | | | | | | | | | | |

Total Number of Pages: 02 **M.Tech**
P1ECBC03

1st Semester Regular/Back Examination 2017-18
INTEGRATED CIRCUIT DESIGN
BRANCH: COMMUNICATION ENGG, COMMUNICATION SYSTEMS, ELECTRO COMM. ENGG, ELECTRO AND TELECOMMUNICATION ENGG, SIGNAL PROCESSING AND COMMUNICATION, SIGNAL PROCESSING AND ENGG, VLSI EMBEDDED SYSTEMS, VLSI EMBEDDED SYSTEMS DESIGN, WIRELESS COMMUNICATION TECH.
Time: 3 Hours
Max Marks: 100
Q.CODE: B921

Answer Question No.1 and 2 which are compulsory and any four from the rest.
The figures in the right hand margin indicate marks.
Assume values wherever missing

Q1 **Answer the following questions:** **(2 x 10)**

a) A 70 nm long transistor has a gate oxide thickness of 12 Å. What is its gate capacitance in (F/µm)?

b) For the nMOS enhancement mode transistor, calculate the drain current for V_G = 3 V, V_S = 1 V, V_D = 4 V, V_{T0} = 1 V. Assume k_n=200µA/V^2.

c) Find the amount of energy required to charge and discharge a capacitive load of the CMOS inverter. Assume load capacitance, C_L = 6 fF and power supply voltage,V_{DD} = 2.5 V. Also, find the dynamic power dissipation of the circuit if the inverter is switched at the maximum possible rate of 2 × τ_p, where τ_p = 32.5 μs

d) If a domino gate input is initially a '1' at the start of evaluation, can it make any other transition during evaluation? Why or Why not?

e) What is a Cascode Amplifier? Enlist one of its uses.

f) What is ATE? What are its main components?

g) Differentiate between Source Memory and Capture Memory.

h) Mention one method by which DC voltage trimming is accomplished in Mixed Signal Testing.

i) What is the range of operation of mm wave IC and Terahertz IC?

j) What is a GNRFET?

Q2 **a)** For a CMOS inverter with the following parameters: V_{DD} = 3V, Vtn = 0.6V, Vtp = −0.82V, k' = 100µA/V^2, µn = 2.2µ: Determine the beta ratio, ß$_n$/ß$_p$, for a midpoint (switching threshold) of V_M = 1.3V. Also Determine the relative device widths, W_p/W_n, for V = 1.3V. **(10)**

b) i) What is the oxide capacitance, C_{ox}, if the gate oxide of an nMOS transistor is 50nm thick? **(10)**

ii) If Cox = 30 nF/cm^2, W=1.5µm and L=0.5µm, what is the gate capacitance, Cg?

iii) If Cg = 1fF and V_{tn} = 0.5V for the nMOS transistor, what is the value of the channel charge, Q_e when V_G=1V?

iv) For pMOS transistor, if Cg = 1fF, Vtp = -0.5V, and VDD=2.5V, what is the value of

the channel charge, Qe when V=1.5V?

Q3 **a)** Draw the small signal equivalent of a simple current mirror. Derive its gain. Enlist the factors affecting the accuracy of Current Mirror. **(10)**

b) What are the different performances parameters of OPAMP? **(10)**

Q4 **a)** Derive the complete small-signal model for an NMOS transistor with I_D= 100 µA, V_{SB}=1 V, V_{DS}= 2 V. Device parameters are φ_f= 0.3 V, W = 10 µm, L = 1 µm, γ = 0.5 $V^{1/2}$, k' = 200 µA/V^2, λ = 0.02 V^{-1}, t_{ox}= 100 Angstroms, ψ_0= 0.6 V, C_{sb0}= C_{db0}= 10 fF. Overlap capacitance from gate to source and gate to drain is 1 fF. Assume C_{gb}=5 fF. **(10)**

b) What is a Cascode Amplifier? Draw its Small signal equivalent. **(10)**

Q5 **a)** Discuss about the different Test and Diagnostic Equipment used in Mixed Signal testing. Enlist some Mixed-Signal Testing Challenges. **(10)**

b) With suitable structures write a brief note on any one of the following. **(10)**

(i) Organic FET

(ii) LDMOS

(iii) HEMT

Q6 **a)** What is the use of Arbitrary Waveform Generators and Waveform Digitizers in Mixed Signal Testing? Use suitable diagrams to aid your answer. **(10)**

b) How Clocking and Synchronization in a mixed-signal tester performed? Illustrate. **(10)**

Q7 **a)** Design a circuit described by the function $Y = \overline{A \cdot (B+C) \cdot (D+E)}$ using CMOS logic. Also find the equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $\left(\frac{W}{L}\right)_p = 5$ for all pMOS transistors and $\left(\frac{W}{L}\right)_n = 2$ for all nMOS transistors. Draw the Layout of Y. **(10)**

b) For a CS stage with R_L= 1kΩ. If I_D = 1mA, $\mu_n C_{ox}$ =100 µA/V^2, W/L=10/0.18, V_{TH} = 0.5 V, and λ = 0, find out the region of operation of the transistor. Let V_{DD}=1.8V. **(10)**