Registration No: | | | | | | | | | | |

Total Number of Pages: 02 **M.Tech**
P1ELBC04

1st Semester Regular Examination 2017-18
INTEGRATED CIRCUIT DESIGN
BRANCH : ELECTRICAL AND ELECTRO ENGG
Time : 3 Hours
Max Marks : 100
Q.CODE : B1013

Answer Question No.1 which is compulsory and any FOUR from the rest.
The figures in the right hand margin indicate marks.
Assume values wherever missing

Q1 **Answer the following questions:** **(2 x 10)**

a) Show graphically that as the bias current, Ibias, decreases in an active load inverter, the gain increases for some time and then it becomes independent of Ibias.
b) Draw the circuit of a cascode with cascode load.
c) Implement a SR Latch using CMOS.
d) What are Mixed Signal Systems? What is an ATE?
e) What is HEMT? Mention one of its applications.
f) What is ATE? What are its main components?
g) Draw the layout diagram for the CMOS logic implementation for the given logical function $Q = \overline{AB(CD + CE) + F}$.
h) Implement a SRAM cell using CMOS logic.
i) Why PMOS is used as pull up network and NMOS as pull down network?
j) What is voltage reference circuit? Write down different techniques used in reference circuits?

Q2 **a)** (i) For a CMOS inverter with the following parameters:$V_{DD} = 3V, Vtn = 0.6V, Vtp = -0.82V, k' = 100\mu A/V^2, \mu_n = 2.2\mu_p$: Determine the beta ratio, ßn/ßp, for a midpoint (switching threshold) of V = 1.3V. Also determine the relative device widths, $Wp/Wn, \text{for } V = 1.3V$. **(10)**
(ii) A pMOS transistor of W=3µm and L=0.6µm has parameters tox= 500nm, surface mobility $\mu_p = 200\ cm^2/V - sec$ and threshold voltage V_{tp} = -0.6V. V_{DD} = 3V. Calculate the transistor transconductance, βp. Also estimate the channel resistance, R_p, at $V_{SG}=V_{DD}$.

b) Define Noise Margins. Derive the Noise Margin for a symmetrical CMOS Inverter. **(10)**

Q3 **a)** Calculate the input and output impedance of a Source Follower. **(10)**

b) Find the voltage gain of the common-source amplifier of Figure Q3 (b) with V_{DD} = 5V, R_D = 5kΩ, k'= $\mu_n C_{ox}$ = 100µA/V^2,W = 50µm,L = 1µm,V_t = 0.8V,L_d = 0,X_d = 0,and λ = 0. Assume that the bias value of V_i is 1 V. **(10)**

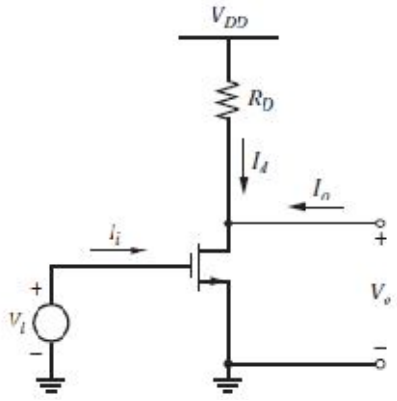

Figure Q3 (b)

Q4 **a)** Explain the concept of Dynamic gate? Explain with an example. What are the issues in Dynamic Design? **(10)**

b) Discuss different types of Current Mirror Circuits. **(10)**

Q5 **a)** Explain datasheets? Explain the different components of test program **(10)**

b) Define line regulation, load regulation, input impedance, and output impedance? Explain DC gain measurement? **(10)**

Q6 **a)** What is FinFET? Discuss its construction and uses. **(10)**

b) Write short notes on Floating gate MOS and Organic FET? **(10)**

Q7 **a)** For a Cascode Amplifier, draw its small signal equivalent and give the value of its V_{bias}. Also calculate its gain. **(10)**

b) How will IC Design impact Internet of Everything? **(10)**