Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech.**
PEE6J001

6th Semester Regular Examination 2017-18
VLSI DESIGN
BRANCH : EEE, ELECTRICAL
Time : 3 Hours
Max Marks : 100
Q.CODE : C350

Answer Part-A which is compulsory and any four from Part-B.
The figures in the right hand margin indicate marks.

Part – A (Answer all the questions)

Q1 **Answer the following questions :** **(2 x 10)**

a) Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?
(a) Simulation (c) Synthesis
(b) Optimization (d) Verification

b) The _____ programming technology is predominantly associated with FPGAs.

c) In enhancement MOSFET, the magnitude of output current _____ due to an increase in the magnitude of gate potentials.
(a) Increases (c) Decreases
(b) Remains constant (d) None of the above

d) Which programming technology/ies is/are predominantly associated with SPLDs and CPLDs?
(a) EPROM (c) EEPROM
(b) Flash (d) All the above

e) _____ is used in logic design of VLSI.

f) The current I_{DS} _____ as V_{DS} increases.

g) Gate capacitance per unit area is scaled by _____.

h) In a PLA _____ are programmable.

i) In a BIST technique ORA and PSBRG uses _____

j) The PLA provides a systematic and regular way of implementing multiple output functions of n variables in
(a) POS form (c) Complex form
(b) SOP form (d) Simple form

Q2 **Answer the following questions : *Short answer type :*** **(2 x 10)**

a) How to calculate the fan-in and fan-out in digital electronics?

b) What are the advantages and disadvantages of FPGAs?

c) Draw the circuit diagram for CMOS two-input NOR Gate.

d) Draw the basic structure of a CMOS domino logic.

e) What is the necessity of clocked sequential circuit in VLSI design?

f) List out the limitations of Constant Field Scaling.

g) Compare CMOS, Bipolar Junction Transistor (BJT) and Gallium Arsenide Technology (GaAs).

h) Give the advantages and disadvantages of cell based design and ASIC design.

i) Why is PMOS good to pass logic 1 and NMOS is good to pass logic 0? Explain?

j) What is the difference between LUT and CLB?

Part – B (Answer any four questions)

Q3 **a)** Explain the p-well CMOS Step by Step Fabrication Processing Technology with neat diagram? **(10)**

b) Compare full custom design with semi custom design styles upon the design cycle time and achievable circuit performance. **(5)**

Q4 **a)** An nMOS transistor is operating in saturation region with the following parameters. V_{gs}=4V, V_{th}=1.1V, W/L=110, $\mu_n C_{ox}$=110μA/V^2. Find Transconductance of the device. **(10)**

b) Explain the term "aspects of MOSFET" in VLSI Design? **(5)**

Q5 **a)** Discuss the inverter delay and propagation delay with neat diagram and derivation? **(10)**

b) Draw the stick diagram and layout diagram for a CMOS 2 input NAND gate. **(5)**

Q6 **a)** What is the need of Testability and explain why do we need DFT (Design For Testability) in a VLSI domain. **(10)**

b) Explain the advantages and disadvantages SoC design. **(5)**

Q7 **a)** Explain two phase clock generator using D- flip-flop and draw the corresponding waveforms? **(10)**

b) Explain CMOS transmission gates? What do you mean by high impedance state? **(5)**

Q8 **a)** Define threshold voltage in CMOS and derive an expression for threshold voltage of a CMOS inverter. Show the VTC and power supply current of a CMOS Inverter circuit. **(10)**

b) What is Dynamic power dissipation in CMOS? **(5)**

Q9 **a)** Consider a CMOS inverter with the following parameters: **(10)**
nMOS $V_{TO,n}$ = 0.8v $\mu_n C_{ox}$=64μA/V^2 $(W/L)_n$=8
pMOS $V_{TO,p}$=-0.9v $\mu_p C_{ox}$=28μA/V^2 $(W/L)_p$=12
Calculate the noise margins and the switching threshold (V_{th}) of this circuit.
The power supply voltage is VDD=3.4V.

b) Explain what are the five electrical parameter characterize level 1 Model equation using SPICE model? Write the SPICE keyword for the above five electrical parameter. **(5)**