Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech**

PCS7J003

7th Semester Regular / Back Examination 2019-20

VLSI DESIGN

BRANCH : CSE

Max Marks : 100

Time : 3 Hours

Q.CODE : HRB023

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.

The figures in the right hand margin indicate marks.

Part- I

Q1 **Only Short Answer Type Questions (Answer All-10)** **(2 x 10)**

a) Differentiate between two types of oxidation process used in IC fabrication.

b) What do you understand by patterning in IC fabrication process?

c) What is dielectric constant value of the commonly used dielectric in MOS gate fabrication.

d) Draw a neatly labelled cross-section layout of a Schottky diode.

e) State the characteristics of self-aligned gate process in IC fabrication process.

f) How latch up problem can be minimized in a CMOS circuit.

g) Why the upper part and lower part of CMOS based circuits are called pull-up and pull-down network respectively?

h) How the transmission gate is able to overcome the limitations of pass transistors?

i) Draw a neat and properly labelled diagram of a BiCMOS based inverter and explain in brief the operation of the circuit.

j) Write down the characteristics of FPGA.

Part- II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) Illustrate the process of ion implantation in vlsi IC fabrication process.

b) Why annealing process is required in the fabrication of ICs? Explain.

c) What is an epitaxial layer? Explain the need of fabrication of epitaxial layer in ICs.

d) Compare and contrast between junction isolation and dielectric isolation.

e) Analyze the variation in threshold voltage of nMOS and pMOS device with doping concentration.

f) Illustrate the fabrication process steps for the fabrication of a monolithic diffused capacitor.

g) Implement the logical equation $Y = (A + C.D).(\bar{B} + C.D) + A.B.D$ using CMOS design style. How many transistors are used in this implementation?

h) Realize a 6:1 multiplexer circuit in transmission gate technology.

i) Write a note on complementary pass transistor logic supported with suitable examples.

j) What is the constraint on the time period of a clock signal while designing digital sequential logical circuits? Explain.

k) What do you understand by scaling of transistors? In the same context, describe the effects on various parameters of the device when constant field scaling is used.

l) Explain in detail the merits and demerits of gallium arsenide technology process over silicon technology process.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3		With the help of suitable diagrams explain, in detail, the steps for fabrication of a n-well CMOS inverter.	**(16)**
Q4		Discuss in detail about monolithic MOS structures including JFET and MOSFET.	**(16)**
Q5		Describe about stick diagram. How does it helps in drawing the layout diagram? Explain by taking the example of full adder circuit.	**(16)**
Q6	**a)**	Draw and explain about positive latches using transmission gates. Draw the timing diagram also.	**(8)**
	b)	Explain the process steps of MESFET fabrication with proper diagrams.	**(8)**