Registration No : | | | | | | | | | | |

Total Number of Pages : 03 **B.Tech**
PEEI5404

8th Semester Regular Examination 2017-18
ANALOG VLSI DESIGN
BRANCH : AEIE, BIOMED, CSE, ECE, EIE, ETC, IEE, IT, ITE
Time : 3 Hours
Max Marks : 70
Q.CODE : C533
Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.
Answer all parts of a question at a place.

Q1 **Answer the following questions:** **(2 x 10)**

a) Consider a CMOS process for which L_{min}=0.8μm, t_{ox}=15nm, μ_n=550 cm^2/V.s, and V_{th}=0.7v. find C_{ox} and K_n'.

b) For the configuration shown in fig-1(b) below, determine the small-signal resistances R_x.

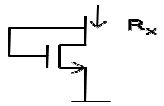

Fig-1(b)

c) With the help of a neat sketch show and explain various terms like channel length(L), lateral diffusion length(L_D), and effective channel length for a MOS transistor.

d) A MOSFET is biased at a drain current of 0.5mA. Draw the low-frequency small-signal equivalent circuit. If μ_nC_{ox}=100mA/V^2,W/L=10 and λ=0.1V^{-1}, calculate its small signal parameter g_m and r_0.

e) For a particular IC fabrication process, the transistor conductance parameter K_n'=50μA/V^2, and V_{th}=1V. In an application in which V_{GS}=V_{DS}=V_{supply}=5V, a drain current of 0.8mA is required of a device of minimum length of 2 mm. What value of channel width must the design use?

f) Why N-MOSFET is faster than P-MOSFET?

g) Common mode rejection ratio(CMRR), ideally it should be infinite for a differential amplifier. Explain, why it becomes finite practically in differential amplifier ?

h) Define channel length modulation. Write down the current expression N-MOSFET with respect to channel length modulation.

i) For MOSFET operating in linear, how g_m and V_{GS}-V_{th} change if both W/L and I_D are doubled?

j) A N-channel MOSFET (K_N=40μA/V^2) has a drain current I_D=4μA. Find the aspect ratio at which the transistor is at subthreshold limit

Q2 **a)** An n-channel MOS device in a technology for which oxide thickness is 20 nm, minimum gate length is 1 μm, K_n'=100μA/V^2, and V_{th}=0.8 V operates in the tride region, with small V_{ds} and with gate-source voltage in the range of 0V to 5 V. what device width is needed to ensure that the minimum available resistance is 1 KΩ? **(5)**

b) The cascode amplifier of fig-2(b) shown below incorporates the following device parameters. $(W/L)_{1,2}=30$, $(W/L)_{3,4}=40$ and $I_{D1}=....=I_{D4}=0.5$ mA. If $\mu_n C_{ox}=100\mu A/V^2$, $\lambda_n=0.1V^{-1}$ and $\lambda_p=0.1V^{-1}$, determine the voltage gain. **(5)**

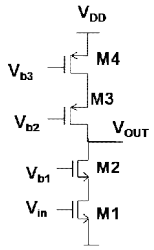

Fig-2(b)

Q3 **a)** Explain the concept of two stage op-amp? Compare the performance of various op-amp topologies (Telescope, Folded cascode, Gain boosted). **(5)**

b) What is a Gilbert cell? Explain why the Gilbert cell can operate as an analog voltage multiplier. **(5)**

Q4 **a)** The differential amplifier circuit shown in fig-4 below uses a resistor $R_X=500\Omega$ rather than a current source to define a tail current I_{TAIL} of 1 mA. Assume $(W/L)_1=(W/l)_2=(25/0.5)$, $\mu_n C_{ox}=50\mu A/V^2$, $V_{th}=0.6$ V, and $V_{DD}=3V$. **(5)**

(I)What is the required input CM for which R_X sustains 0.5V?

(II) Calculate R_D for a differential gain of 5.

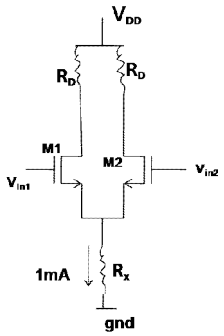

Fig-4

b) What happens at the output if the CM level is 50 mV higher than the value calculated at Q4 (a) above? **(5)**

Q5 **a)** Why we need a current mirror circuit? Discuss in detail about Wilson current mirror circuit. **(5)**

b) Draw a cascode current mirror circuit. Discuss its frequency responses. **(5)**

Q6 **a)** Draw and explain the circuit diagram of colpitts oscillator and derive its frequency of oscillation. **(5)**

b) What is a Gilbert cell? Explain why the Gilbert cell can operate as an analog voltage multiplier. **(5)**

Q7 **a)** Discuss the design and tuning in ring oscillator . **(5)**

b) For an OPAMP, define the following terms.(I) slew rate, (II) CMRR, (III)Input offset voltage, (IV) Output Offset voltage,(V)Bias current **(5)**

Q8 **Write short answer on any TWO :** **(5 x 2)**

a) Active current mirrors

b) Slew rate and power supply rejection.

c) Cascode stage in a single stage amplifier

d) Voltage controlled oscillator (VCO)