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Total Number of Pages: 04

M.TECH
VLPC101

1st Semester M.Tech Regular/ Back Examination 2015-16

HDL and High Level Synthesis

Branch: VLSI& Embedded Sytems

Time: 3 Hours

Max marks: 70

Question Code:T1192

Answer Question No.1 which is compulsory and any five from the rest.

The figures in the right hand margin indicate marks.

(2 x 10)

Q1 Answer the following questions:

a) What is a Hardware Description Language? How is it different from a normal programming language?

b) Given

SIGNAL a : BIT := '1';

SIGNAL b : BIT_VECTOR (3 DOWNTO 0) := "1100";

SIGNAL c : BIT_VECTOR (3 DOWNTO 0) := "0010";

Fill up the following blanks:

x1 <= a & c; x1<=_____

x2 <= b sll 2; x2<=_____

c) Enlist some concurrent and some sequential statements of VHDL. (Atleast two each).

d) Give examples of a block statement. What is a guarded block?

e) (i) There are two functions with the same name. Which feature of VHDL does this exemplify?

(ii) Given two functions:

function check_limit(value : integer) return boolean;--function 1

function check_limit(value : word_32) return boolean;--function 2

Now if we call these functions by the following statements

test1 := check_limit(4095)

test 2:= check_limit(X"0000_0FFF")

Identify which function will be called when.

f) Differentiate between Sequential Signal assignment statements and Concurrent Signal Assignment statements.

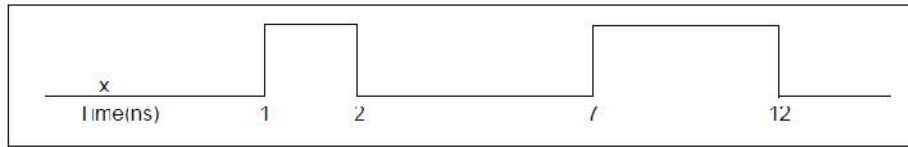
g) Differentiate between Identifier and reserved word with example.

h) 5 Waveform of signal X is given below .Sketch the waveform for Y and Z for

following assignment.

Y <= transport X after 2ns;

Z <= X after 2ns;



i) Differentiate between port mapping by name and port mapping by position.

j) Give the enumeration type definition for a four-valued system 0, 1, X, Z.

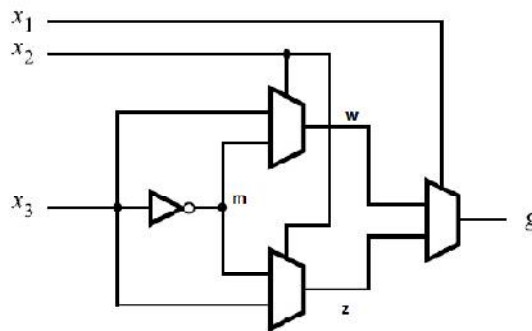
Q2 a) Find at least five errors in the following code: (5)

```

Library ieee;
Use ieee.std_logic_1164.all;
Entity Q2 is
ports( DATA : in std_logic_vector(7..0);
CARRY :in std_logic;
result :out BIT);
end Q2;
architecture Q2 of Behavioral is
signal MODE : std_logic_vector(3 downto 0);
begin
MODE => DATA(6 downto 4);
With MODE select
RESULT <= CARRY when "0000",
'1' when "0001",
'0' when "1000";
Y <= CARRY and result;
End Behavioral;

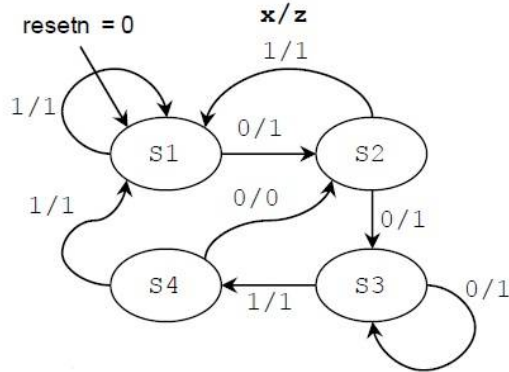
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b) Write a VHDL description of the following circuit. Derive the logic function g represented by the circuit. (5)



Q3 a) Write VHDL code that represents a T flip-flop with an asynchronous clear input. Use behavioral code, rather than structural code. (5)

b) Write the VHDL code for the given state machine. (5)



Q4 Suppose that the operations that we want to implement in an ALU are as defined in Table below. The xi column shows the values that the output, LE must generate for the different operations. The yi column shows the values that the output, AE must generate. The c0 column shows the carry signals that the output, CE must generate. Implement this ALU using VHDL. (10)

s_2	s_1	s_0	Operation Name	Operation	x_i (LE)	y_i (AE)	c_0 (CE)
0	0	0	Pass	Pass A to output	a_i	0	0
0	0	1	AND	A AND B	a_i AND b_i	0	0
0	1	0	OR	A OR B	a_i OR b_i	0	0
0	1	1	NOT	A'	a_i'	0	0
1	0	0	Addition	$A + B$	a_i	b_i	0
1	0	1	Subtraction	$A - B$	a_i	b_i'	1
1	1	0	Increment	$A + 1$	a_i	0	1
1	1	1	Decrement	$A - 1$	a_i	1	0

Q5 a) Make a Comparison between the VHDL Constructs-WHEN and CASE by taking a 2-to-4 decoder circuit as an example. (5)

b) Discuss the Simulation System in CAD design with suitable block diagrams. (5)

Q6 a) Complete the timing diagram of the circuit whose VHDL description is shown below. Also draw the circuit. (5)

```

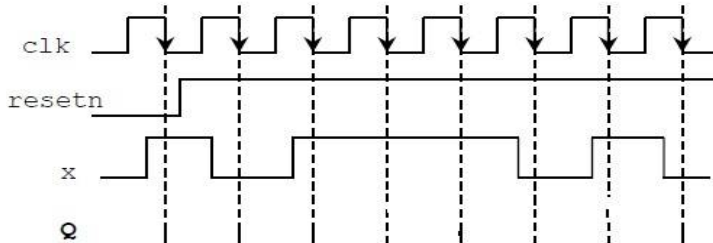
library ieee;
use ieee.std_logic_1164.all;
entity circ is
port ( resetn, x, clk: in std_logic;
      q: out std_logic);
end circ;
architecture a of circ is
signal qt: std_logic;
begin
process (resetn, clk, x)
begin
if resetn = '0' then
qt <= '0';

```

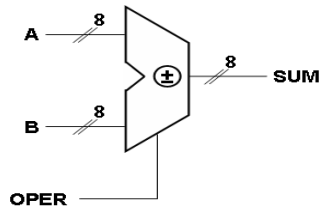
```

elseif (clk'event and clk = '0') then
if x = '1' then
qt <= not(qt);
end if; end if;
end process;
q <= qt;
end a;

```



- b) An unsigned 8-bit Adder/Subtractor is shown in the Figure below. Write the VHDL codes for this unsigned 8-bit Adder/Subtractor. (5)



I/O Pins	Description
A, B	Add/Sub Operands
OPER	Add/Sub Select
SUM	Add/Sub Result

- Q7 a) Draw the logic diagram and write VHDL structural model code for 4-bit binary comparator. (5)

- b) Consider the VHDL process shown below. (5)

```

process (a, b, c) begin
x <= a and b;
if a < b then
y <= b + c;
elsif b > c then
x <= a xor c; y <= '1';
else
y <= a;
end if;
end process;

```

Draw a circuit directly from the VHDL that implements this process (do not derive simplified equations for this part). Your circuit may include XOR gates and 2:1 MUXs.

- Q8 Write Short Notes on any two of the following: (5 X 2)

- The ASIC Design Process.
- CAD tools and its functions
- Datapath-Controller design
- 32 bit ROM implementation
- Functions and Procedures