Registration No : | | | | | | | | | | |

Total Number of Pages : 01 **MCA**
MCC202

2rd Semester Back Examination 2018-19
COMPUTER ORGANISATION AND SYSTEM ARCHITECTURE
BRANCH : MCA
Time : 3 Hours
Max Marks : 70
Q.CODE : F239

Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.

Q1 **Answer the following questions :** **(2 x 10)**

a) Wirite down the basic concepts of VonNeuman Architecture?
b) Differentiate between SRAM and DRAM.
c) State the types of registers used in the microprocessor.
d) Write down the different types of interrupts.
e) Define CLV.
f) With an example state auto-increment addressing mode.
g) Determine $(110110)_2$- $(10110)_2$.
h) How the cache coherency is eliminated?
i) Differentiate between Memory mapped I/O and I/O mapped I/O.
j) What is Seek time and Latency time?

Q2 **a)** Explain different types of addressing modes with suitable example. **(5)**
b) Simplify the following Boolean function in product-of-sums form by means of a four-variable map. **(5)**

$$F(w,x,y,z)=\sum(2,3,4,5,6,7,11,14,15)$$

Q3 **a)** With a suitable diagram explain the data flow of Instruction Cycle **(5)**
b) What is Instruction Format? Describe about three address, two address and one address instruction with example. **(5)**

Q4 **a)** Draw a flow chart for Booth's algorithm. Multiply 10111 by 10011 using Booth algorithm. **(5)**
b) Explain the benefits of using a multibus architecture compared to single bus architecture. **(5)**

Q5 **a)** Explain the concept of array processor. How parallel processing is achieved with the help of pipelining? **(5)**
b) Differentiate between RISC and CISC. **(5)**

Q6 Discuss the concept of mapping function. Evaluate the different types of mapping function in case of cache memory. **(10)**

Q7 Describe the working of micro-programmed CPU with suitable diagram. With suitable block diagram explain the data transfer using DMA controller. **(10)**

Q8 **Write short answer on any TWO :** **(5 x 2)**

a) Cache wire policy
b) Flynn's classification
c) Interrupt driven I/O