Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **MCA**
MCC202

2nd Semester Back Examination 2017-18
COMPUTER ORGANISATION AND SYSTEM ARCHITECTURE
BRANCH : MCA
Time : 3 Hours
Max Marks : 70
Q.CODE : C718

Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.
Answer all parts of a question at a place.

Q1 **Answer the following questions :** **(2 x 10)**

a) Differentiate between SIMD & MIMD.

b) Draw the memory hierarchy diagram by considering speed and cost per bit.

c) Formulate address for a memory, consisting of 256 memory module and each of 1KB?

d) Differentiate between microinstruction & micro-operation.

e) How many 256k*4 chips are required to create a 4MB memory?

f) Differentiate unified cache and split cache with advantages and drawbacks.

g) What is baised exponent? What is the significance of using baised exponent?

h) What is mantissa alignment and normalized result in floating point number?

i) How many clock cycles are required to process 5 instructions in a 6 segment instruction pipeline?

j) What is attached array processor? Why it is named so?

Q2 Explain Delayed LOAD & Delayed Branch processing In RISC pipeline and how delayed load & delayed branch are handled in RISC pipeline. Differentiate RISC processor & CISC processor. **(10)**

Q3 Explain Synchronous & asynchronous data transfer in detail. What are the advantages of IO interface? **(10)**

Q4 **a)** Multiply +29 by -15 using booth algorithm multiplication. **(5)**

b) What is address mapping? Differentiate between memory mapped IO and IO mapped IO. **(5)**

Q5 **a)** Describe characteristics, read & write mechanism, data organization & formatting in magnetic disk. **(6)**

b) Describe direct, indirect and register indirect addressing mode with example. **(4)**

Q6 **a)** In direct mapping, consider a cache memory of 64KB and main memory of 8MB and each block of main memory is of 8byte. Find the size of tag field, line field & word field. Find no. of lines in cache memory and no. of blocks in main memory. **(5)**

b) Describe set associative mapping technique in cache memory. **(5)**

Q7 **a)** Describe different mapping techniques in virtual memory. What are the advantages of associative memory mapping technique? **(5)**

b) Find the total no. of page faults for the string 0,1,2,3,1,2,4,0,5,3,1,6 using FIFO,LRU & optimal algorithm if no. of blocks in main memory is 3. **(5)**

Q8 **Write short notes on any TWO :** **(5 × 2)**

a) Instruction cycle

b) Hardwired control unit

c) Addition and subtraction of fixed point signed number

d) Locality of reference