www.bputonline.com

Registration No: | | | | | | | | | | |

www.bputonline.com

Total Number of Pages:02

B.TECH
PEI4G001

4th Semester Minor Examination 2016-17
Digital Electronic Circuits
BRANCH: AEIE, EIE, IEE
Time: 3 Hours
Max Marks: 100
Q.CODE: Z1112

Answer Part-A which is compulsory and any four from Part-B.
The figures in the right hand margin indicate marks.

Part – A (Answer all the questions)

Q1 Answer the following questions: ***multiple type or dash fill up type*** **(2 x 10)**

a) Convert $(634)_8$ to binary.
b) A number system with radix 16 is called_____.
c) A 32x10 ROM contains a _____ decoder.
d) For the PAL design of a logic circuit, a single literal term

i) Requires an AND gate
ii) Does not require an AND gate
iii) Requires an AND gate and one input for OR gate
iv) Requires an inverter

e) Which of the following is the fastest logic
(A) TTL (B) ECL (C) CMOS (D) LSI
f) Convert $(10111)_2$ to Gray code.
g) What is propagation delay?
h) Write any two non-weighted codes.
i) The output frequency of a mod-10 counter is 6kHz. Find its input frequency?
j) $(1111101111011110)2 = (\quad)_{16}$

bput question papers visit http://www.bputonline.com

Q2 Answer the following questions: ***Short answer type*** **(2 x 10)**

a) State De Morgan's theorem and absorption property.
b) Explain the difference between flip-flops and latch?
c) Subtract binary number 0100111 from 01011000 using 1's complement.
d) What is a PAL? Give an example.
e) Define resolution and accuracy of DACs.
f) What is the difference between shift registers and counters?
g) Write the Boolean output function(Y) of a 4:1 mux with $I_0=I_1=A$ and $I_2=I_3=\bar{A}$
h) What is programmable logic array? How it differs from ROM?
i) The propagation delay for each flip-flop is 50 ns. Determine the maximum operating frequency for MOD - 32 ripple counter?
j) Why is multiplexer called a data selector?

www.bputonline.com

Part – B (Answer any four questions)

Q3 **a)** Using K-map method, obtain the minimal sum of product expression of the following function **(6+4)**

$Y=\Sigma(0,2,3,6,7,8,10,11,12,15)$ www.bputonline.com

Draw a logic circuit the following function using NAND gate.

$Y=A+BCD'$

b) Minimize and design the function $f(A,B,C,D)=\Sigma(0,1,3,5,7,8,9,10,11,12,14)$ using K-map. **(5)**

Q4 **a)** Implement following function using a 4:1 multiplexer **(5+5)**

$F(A,B,C)=\Sigma(1,3,5,6)$

b) What do you mean by positive logic and negative logic? Show that a positive logic NAND gate is a negative logic NOR gate and vice versa **(5)**

Q5 **a)** Draw the circuit diagram of a Master-slave J-K flip-flop using NAND gates. What is race around condition? How is it eliminated in a Master-slave J-K flip flop? **(10)**

b) Design a shift left SISO register using D Flip Flops. **(5)**

Q6 **a)** i) Design a 32:1 mux using two 16:1 mux and one 2:1 mux modules. **(6+4)**
ii) Design a full adder circuit using only NAND gate.

b) Design a 4-bit binary subtractor circuit. **(5)**

Q7 **a)** Design a sequential detector which produces an output 1 every time the input sequence 1011 is detected. **(10)**

b) Write a short note on ROM and RAM **(5)**

Q8 **a)** Given a 128x8 ROM chip with an enable input, show the external connections necessary to construct a 512x8 ROM with four chips and a decoder. **(7)**

b) Design a Mod-10 synchronous UP counter using D-flip flop. **(8)**

Q9 **a)** Design a combinational circuit that gives a binary output equal to the square of binary-coded decimal numbers 0 through 9 using ROM. **(10)**

b) Explain the operation of NAND gate using CMOS logic with proper circuit diagram. **(5)**

bput question papers visit http://www.bputonline.com